APPLICATION

FOR

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TITLE: ACTIVE PIXEL SENSOR WITH MIXED ANALOG AND DIGITAL SIGNAL INTEGRATION

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ACTIVE PIXEL SENSOR WITH MIXED ANALOG AND DIGITAL SIGNAL INTEGRATION

Background

Active pixel sensors are well known in the art. A basic description of the active pixel sensors found in U.S. Patent No. 5,471,515, the disclosure of which is incorporated by reference to the extent necessary for proper understanding.

An active pixel sensor, and many other image sensors, have inherent trade-offs. Typically, the trade-off is made between sensitivity, versus motion resolution, versus space resolution.

For example, we obtain sensitivity by increasing the integration time. However, with a higher integration time, motion becomes more choppy, and hence motion sensitivity is decreased. Sensitivity can also be increased by increasing the pixel size. However, space resolution then decreases, again supporting the trade-off.

Integrated circuit designers continually attempt to put more circuitry on a chip. Lines on the chip are becoming smaller: for example, current technology may use a 0.11 micron process for digital circuitry. However, the image sensor, which is effectively analog, may be subject to a physical minimum size. A pixels that has too small a size and/or high gain, would have

insufficient capacitance to allow the sensor to obtain the signal to noise ratio required for quality image acquisition.

Summary

The inventor recognized that memory size can form an effective tradeoff against pixel size. The present specification describes receiving information in an analog photosensor array, and integrating that information in on-chip digital memory. According to this system, an analog array is placed on the same substrate with a digital memory. The information from the analog array is sampled periodically, and the integration is carried out in the digital memory.

Brief Description of the Drawings

Figures 1 shows a basic block diagram; and

Figures 2 and 3 respectively show more detailed block diagrams of the circuitry.

Description of the Preferred Embodiments

The basic system is shown in FIG. 1. An analog image detector 100, preferably a CMOS image sensor, reads out the image at some time period, e.g., between 1 microsecond and 1 millisecond. Each pixel is coupled to a digital memory 110.

Digital memory integrates the instantaneous information received from the pixels.

clno.C17 Current frame times are preferably either 33 milliseconds for a 30-frame per second system, or 16 milliseconds for high motion resolution of 60 milliseconds.

In addition to the other advantages noted above, this architecture allows pixel capacitance to be reduced and pixel gain to be increased, since the pixel need provide only instantaneous values, and does not need to integrate the incoming charge.

The signal integration process is divided into two parts: an analog part in the active pixel sensor 100 and a digital part in digital random access memory.

A first embodiment is shown in FIG. 2. Fig. 2 shows the active pixel sensor array 100, coupled with an analog signal processor 202, column A/D converters 204, and a digital signal processor 206. The analog signal processor 202 includes column analog double sampling circuitry both signal and reference to decrease the pixel fixed pattern noise. Preamplifiers, with adjustable gains, can also be used to increase the sensitivity and provide an automatic exposure control, as is known in the art.

The system as described herein uses column parallel A/D conversion, where one separate A/D converter is provided for each

column of the active pixel sensor array. In this system, digital integration may be used for oversampling the A/D converter. Digital sampling can reduce the quantization noise density, and hence increase the effective resolution of the system proportionally to arise of the frame bit. Preferably the system operates with an AC input noise of about half of the least significant bit.

The digital signal processor 206 provides arithmetic operations such as addition, subtraction, division, and multiplication, and also includes a buffer memory to maintain intermediate results. DSP 206 can also act to digitally correct column digital fixed pattern noise. FIG. 3 shows a system similar to that in FIG. 2 but with twice as many digital arrays and processing circuits.

In operation, the sensor is preferably a CMOS image sensor that is of a sufficiently small size that it cannot integrate for a desired frame period. The information from the sensor is sampled by the column A/D converters at an oversampled rate. Each sample is stored in the digital memory array, and the values are integrated in that memory. A digitally integrated value can be subsequently read from the digital memory array.

Although only a few embodiments have been disclosed in detail above, other modifications are possible in the preferred embodiment.